What Is Claimed Is:

1. A method of forming a memory cell with a single sided buried strap, comprising the steps of:

providing a substrate having a trench;

forming a trench capacitor at a lower portion of the trench;

forming a collar insulating layer on a sidewall of an upper portion of the trench;

forming a first conductive layer above the trench capacitor and filling the trench;

removing part of the first conductive layer and part of the collar insulating layer to form a remaining first conductive layer and a remaining collar insulating layer in an opening, wherein the opening has a first sidewall and a second sidewall, and a top surface of the remaining collar insulating layer is lower than that of the remaining first conductive layer;

performing an angle implantation with fluorine-containing ions on the first sidewall of the opening;

performing a thermal oxidation process to form a first oxide layer on the first sidewall and a second oxide layer on the second sidewall, wherein a thickness of the first oxide layer is greater than that of the second oxide layer;

removing the second oxide layer to expose the second sidewall; and

forming a second conductive layer serving as a buried strap at a bottom of the opening, wherein the second conductive layer is insulated from the first sidewall by the first oxide layer.

2. The method according to claim 1, further comprising the steps of:

forming an insulating layer on the second conductive layer;

forming a gate insulating layer on the second sidewall;

forming a gate in the opening; and

forming a source region and a drain region in the substrate.

3. The method according to claim 1, wherein the formation of the trench comprises the steps of:

forming a patterned pad layer on the substrate; and

using the pad layer as a mask, removing part of the substrate to form a trench in the substrate.

4. The method according to claim 1, wherein the substrate is a silicon substrate.

5. The method according to claim 3, wherein the pad layer comprises an oxide pad layer and a nitride layer.

6. The method according to claim 1, wherein the collar insulating layer is a SiO_2 layer.

7. The method according to claim 1, wherein the first conductive layer is a doped polysilicon layer.

8. The method according to claim 1, wherein the fluorine-containing ions comprise F and/or BF_2 ions.

9. The method according to claim 1, wherein an implantation energy of the angle implantation is 15~30keV.

10. The method according to claim 9, wherein a dosage of the angle implantation is 1E14~4.5E15 ions/cm^2.

11. The method according to claim 1, wherein an operating temperature of the thermal oxidation process is 900~950°C.

12. The method according to claim 1, wherein the second conductive layer is a doped polysilicon layer.

13. The method according to claim 2, wherein the gate oxide layer is a SiO_2 layer formed by thermal oxidation.

14. The method according to claim 13, wherein an operating temperature of the thermal oxidation process is 800~1000°C.

15. A method of forming a memory cell with a single sided buried strap, comprising the steps of:

providing a substrate;

forming a patterned pad layer on the substrate;

using the pad layer as a mask, removing part of the substrate to form a trench therein;

forming a trench capacitor at a lower portion of the trench;

forming a collar insulating layer on a sidewall of an upper portion of the trench;

forming a first conductive layer above the trench capacitor and filling the trench;

removing part of the first conductive layer to a determined depth, thus forming a remaining first conductive layer;

removing part of the collar insulating layer to form a remaining collar insulating layer in an opening, wherein the opening has a first sidewall and a second sidewall, and a top surface of the remaining collar

insulating layer is lower than that of the remaining first conductive layer;

performing an angle implantation with fluorine-containing ions on the first sidewall of the opening;

performing a thermal oxidation process to form a first oxide layer on the first sidewall and a second oxide layer on the second sidewall, wherein a thickness of the first oxide layer is greater than that of the second oxide layer;

removing the second oxide layer to expose the second sidewall; and

forming a second conductive layer serving as a buried strap at a bottom of the opening, wherein the second conductive layer is insulated from the first sidewall by the first oxide layer;

forming an insulating layer on the second conductive layer;

forming a gate insulating layer on the second sidewall;

forming a third conductive layer serving as a gate in part of the opening;

forming an insulating spacer on the sidewall of the opening;

forming a fourth conductive layer to fill the opening;

forming a fifth conductive layer on the fourth conductive layer; and

forming a source region and a drain region in the substrate.

16. The method according to claim 15, wherein the substrate is a silicon substrate.

17. The method according to claim 15, wherein the fluorine-containing ions comprise F and/or BF_2 ions.

18. The method according to claim 15, wherein an implantation energy of the angle implantation is 15~30keV and a dosage of the angle implantation is 1E14~4.5E15 ions/cm^2.

19. The method according to claim 15, wherein an operating temperature of the thermal oxidation process is 900~950°C.

20. The method according to claim 15, wherein the gate oxide layer is a SiO_2 layer formed by thermal oxidation.